Electronic Version
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Claims

[c1] 1. A NAND flash memory cell row, comprising:

a substrate;

a plurality of first stacked gate structures disposed on the substrate, wherein each of the first stacked gate structures comprises an erase gate dielectric layer, an erase gate and a first cap layer;

two second stacked gate structures disposed on the substratebeside two outer sides of the first stacked gate structures respectively, wherein each of the second stacked gate structurescomprises a select gate dielectric layer, a select gate and a second cap layer;

a plurality of control gates disposed between the first stacked gate structures and each of the second stacked gate structures, and between every two of the neighboring first stacked gate structures;

a plurality of floating gates disposed between the control gates and the substrate, wherein each of the floating gates has sharp corners and a concave surface facing each of the control gates, and the edge of the concave surface is lower than a top surface of the erase gate;

an inter-gate dielectric layer disposed between each of the control gates and each of the floating gates;

a tunnel oxide layer, disposed betweeneach of the floating gates and the substrate, between each of the floating gates and the first stacked gate structures, and between each of the floating gates and the second stacked gate structures;

a plurality of doping regions disposed in the substrate under the first stacked gate structures; and

a plurality of source/drain regions disposed in the exposed substrate outside the second stacked gate structures.

[c2] 2.The NAND flash memory cell row of claim 1, wherein a material of the tunnel oxide layer comprises a silicon oxide.

[c3] 3.The NAND flash memory cell row of claim 1, wherein the inter-gate dielectric layer comprises a material selected from the group consisting of silicon oxide/silicon nitride/silicon oxide, silicon nitride/silicon oxide and silicon oxide/silicon nitride.

[c4] 4. The NAND flash memory cell row of claim 1, wherein the first and the second cap layers comprise an oxide layer and a dielectric layer disposed on the oxide layer.

[c5] 5. The NAND flash memory cell row of claim 1, wherein the NAND flash memory cell further comprising:

a p-type well region disposed in the substrate, wherein a depth of the p-type well region is deeper than a depth of the source/drain regions.

[c6] 6. Amanufacturing method of a NAND flash memory cell row, comprising:
forming a plurality of doping regions and a plurality of source/drain regions in a substrate, wherein the source/drain regions aredisposed at outer sides of the doping regions;
forming a plurality of stacked gate structures on the substrate,wherein someof the stacked gate structuresare disposed on the doping regions and eachof the stacked gate structures comprises at least an erase gate, and someof the stacked gate structuresare disposed at a distance from the doping regions and beside the source/drain regions and eachof the stacked gate structures comprises at least a select gate;
forming a tunnel oxidelayer on the substrate to cover the substrate, the erase gate and the select gate surface;
forming a plurality of floating gates between the stacked gate structures, wherein a top surface of the floating gatesis a concave surface and has a sharp edge, wherein an edge of the concave surface is lower than a top surface of the erase gates;
forming an inter-gate dielectric layer onthe floating

gates; and
forming a plurality of control gates on the inter-gate dielectric layer.

[c7] 7.The manufacturing method of NAND flash memory cell row of claim 6, wherein the step of forming the floating gates between the stacked gate structures comprises:
forming a first conductive layer between the stacked gate structures;
removing a portion of the first conductive layer to make a top surface of the first conductive layer is lower than a topsurface of the stacked gate structures;
oxidizing the top surface of the first conductive layer to form an oxide layer on the top surfaceof the first conductive layer; and
removing the oxide layer to form the floating gates.

[c8] 8.The manufacturing method of the NAND flash memory cell row of claim 7, wherein a method of oxidizing the top surface of the first conductive layer comprises a wet oxidation method.

[c9] 9. The manufacturing method of the NAND flash memory cell row of claim 7, wherein a method of removing the portion of the first conductive layer comprises an etch back method.

[c10] 10. The manufacturing method of the NAND flash memory cell row of claim 6, wherein the step of forming the control gates between the stacked gate structures comprises:
forming a second conductive layer on the substrate; and removing a portion of the second conductive layer tillthe top surface of the stacked gate structures are exposed.

[c11] 11. The manufacturing method of the NAND flash memory cell row of claim 10, wherein a method of removing the portion of the second conductive layer comprisesan etch back method or a chemical mechanical polishing (CMP) method.

[c12] 12.The manufacturing method of the NAND flash memory cell row of claim 6, wherein a material of the tunnel oxide layer comprises silicon oxide.

[c13] 13.The manufacturing method of the NAND flash memory cell row of claim 12, wherein a method of forming the tunnel oxide layer comprises a thermal oxidation method.

[c14] 14.The manufacturing method of the NAND flash memory cell row of claim 6, wherein theinter-gate dielectric layer comprises a material selected from the group consisting of silicon oxide/silicon nitride/silicon oxide, sili-

con nitride/silicon oxide or silicon oxide/silicon nitride.

[c15] 15.The manufacturing method of the NAND flash memory cell row of claim 6, wherein the step of forming the stacked gate structureson the substrate comprises:
forming a first dielectric layer, a third conductive layer, an oxide layer and a second dielectric layer on the substrate sequentially; and
patterning the second dielectric layer, the oxide layer, the third conductive layer and the first dielectric layer so as to form a first cap layer, the erase gate and an erase gate dielectric layer on the doping regions, and to form a second cap layer, a select gate and the select gate dielectric layer ata distance from the doping regions and beside a side of the source/drain regions.

[c16] 16.The manufacturing method of NAND flash memory cell row of claim 15, wherein a method of forming the first dielectric layer on the substrate comprises thermal oxidation process.